Redefining Connectivity: Charting Next-Gen Pathways in Chiplet Interconnects

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AI Hardware and Edge AI Summit
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Delivering Custom Silicon in the Data Centre

Customised compute and connectivity reliant on chiplets

Networking

Compute CPU

Custom xPUs

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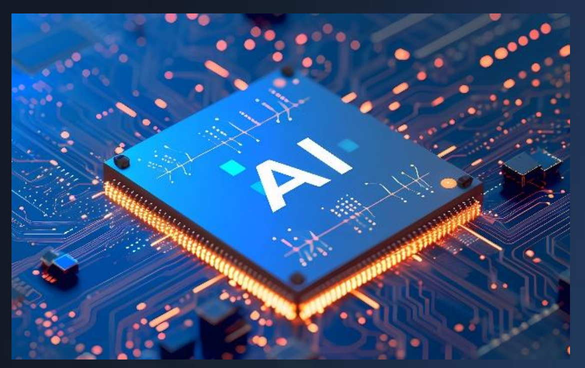
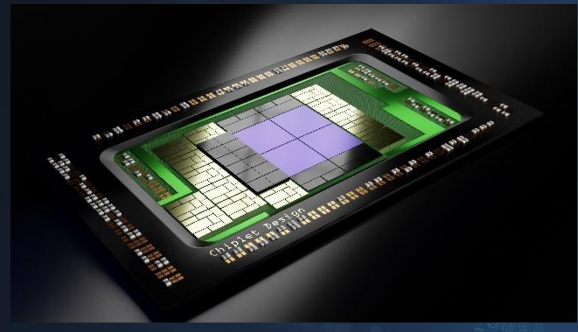
Outline



- Scaling AI with Connectivity



- The Role of Chiplets for AI Compute

- Enabling a Chiplet Ecosystem

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Scaling AI with Connectivity

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Evolving Data Centre Connectivity Landscape

Switches

Compute Servers

- Optical and electrical links
- Flexible and redundant networking

This evolution is accelerating and diversifying with AI deployment in the data centre

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AI in the Data Centre – Proliferating Connectivity

Front-End Data Centre Network

AI Cluster

Back-End ML Network

- Low-latency & high-speed

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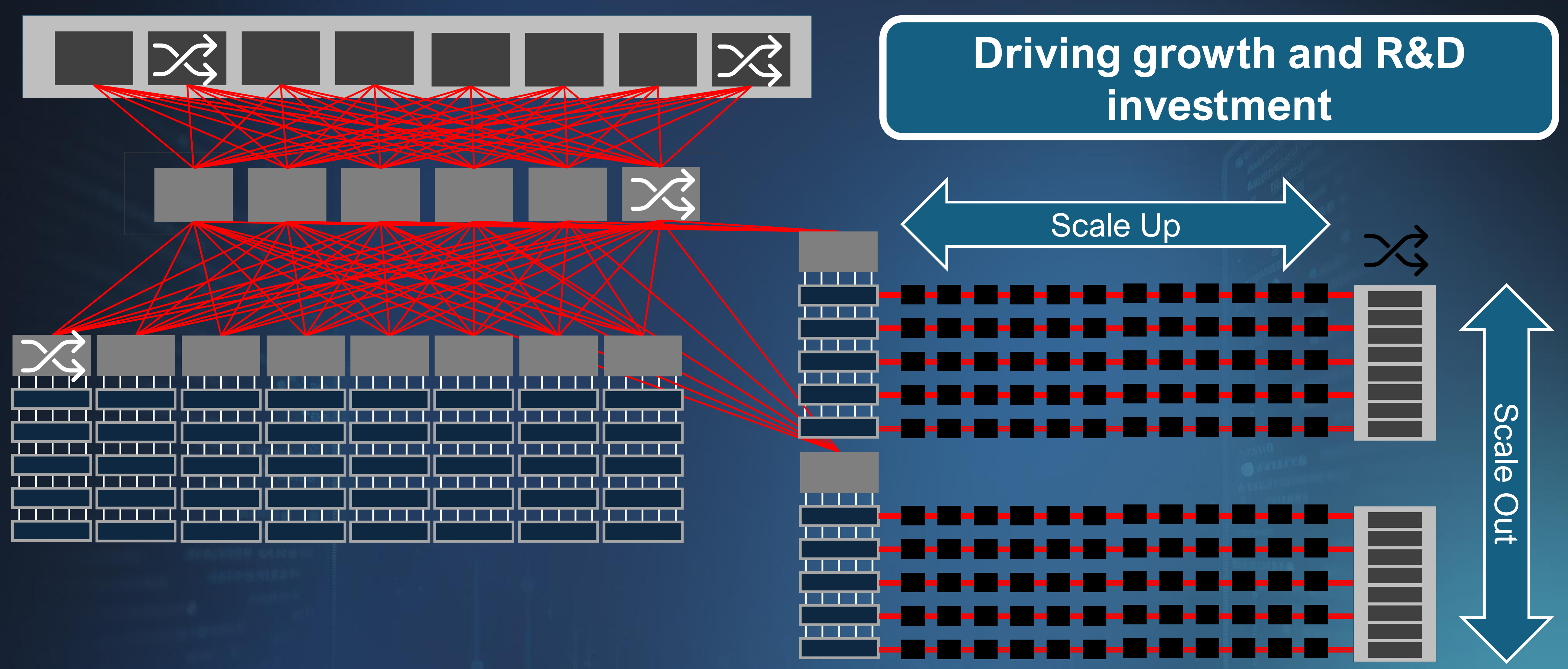
Scaling Up and Out



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Distributed AI

- Data security & privacy
- Energy efficiency
  - ➢ Relies heavily on connectivity

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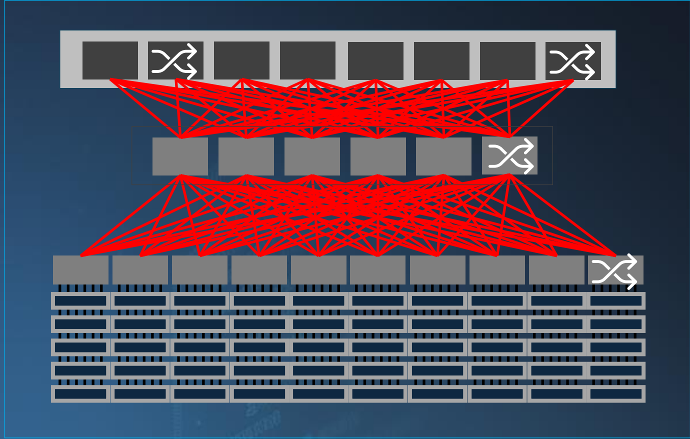
Connectivity Demands for AI

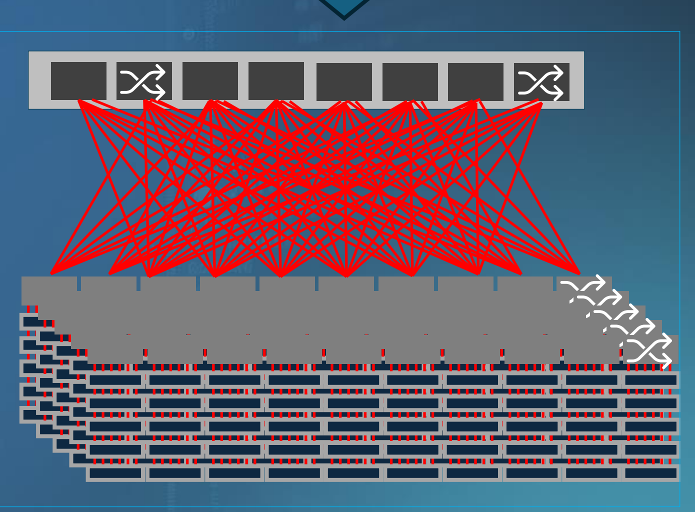
Higher per-lane data rates

Scale up and out to larger clusters

Low latency; Low power; Low failure rate

Proliferation of new optical connectivity technologies





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The Role of Chiplets for AI Compute

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Monolithic Solutions

Benefits and Drawbacks

- Requires integration of external IP
  - Design and verification time and risk
  - Licensing cost
- Maximum size is limited by reticle
- Yield reduced by large die size
- I/O must be in the most advanced technology
- Every I/O must be capable of driving any interconnect

Memory
Memory
HBM
HBM
I/O
I/O
I/O
I/O
Logic
I/O
I/O
I/O
I/O
HBM
HBM
Memory
Memory

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Bandwidth Density

- Reticle-limited die sizes afford roughly 50mm die edge on the east + west
  - ➢ 50Tbps aggregate I/O bandwidth requires 1 Tbps/mm

Adv. Logic Node

Chiplet-Optimized Node

Memory
Memory
HBM
HBM
I/O
I/O
I/O
I/O
Logic
I/O
I/O
I/O
I/O
HBM
HBM
Memory
Memory

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Chiplets

- Reduced design time, risk, NRE and silicon costs
- Composability

Adv. Logic Node

Chiplet-Optimized Node

Memory
Memory
HBM
HBM
Logic
Logic
Logic
Logic
UCIe
I/O
HBM
HBM
Memory
Memory

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Accelerating Hardware Upgrades

- Reduced design time
- Reduced risk

Die-to-Die Interfaces Required for the Chiplet Era

- Composability
- Reduced NRE + Silicon Cost

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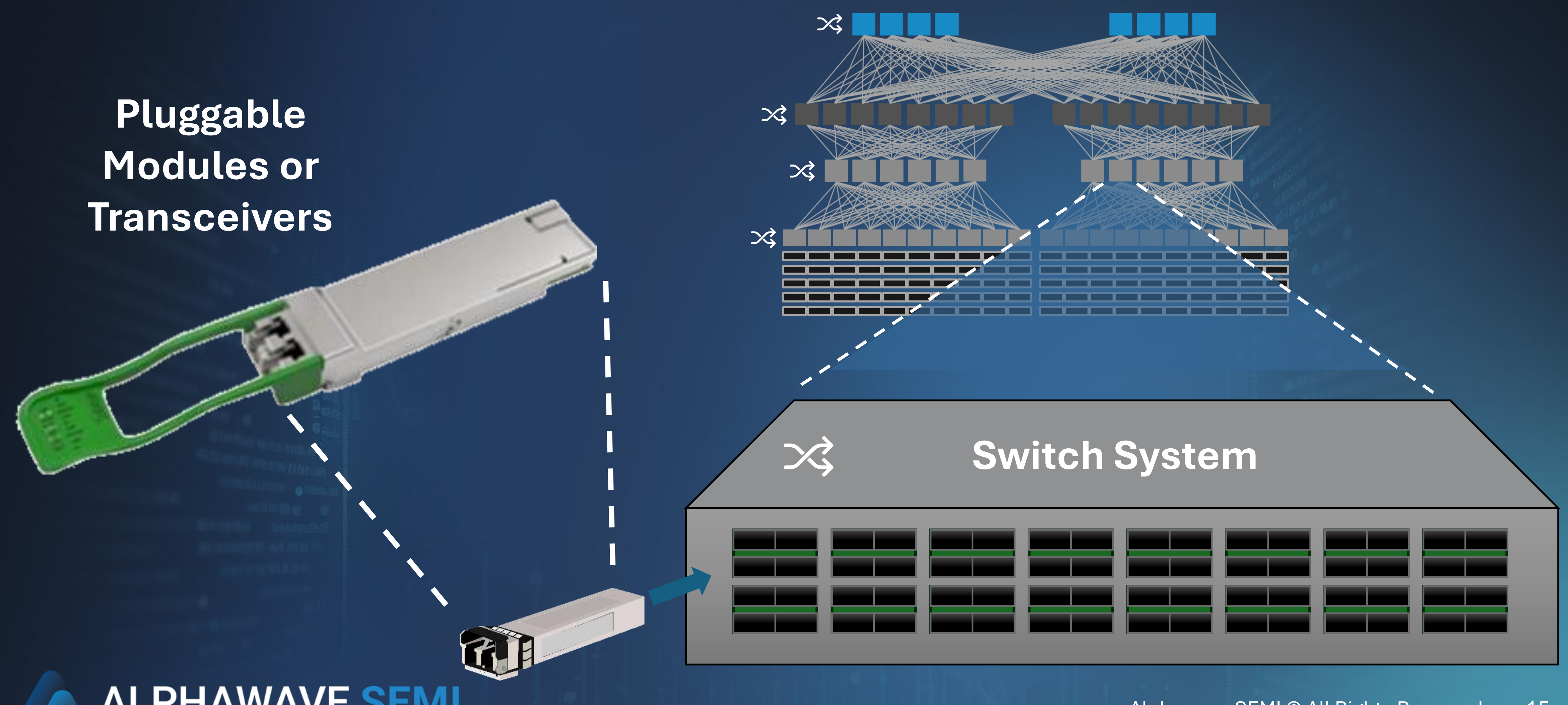
Connectivity Hardware in the Datacenter



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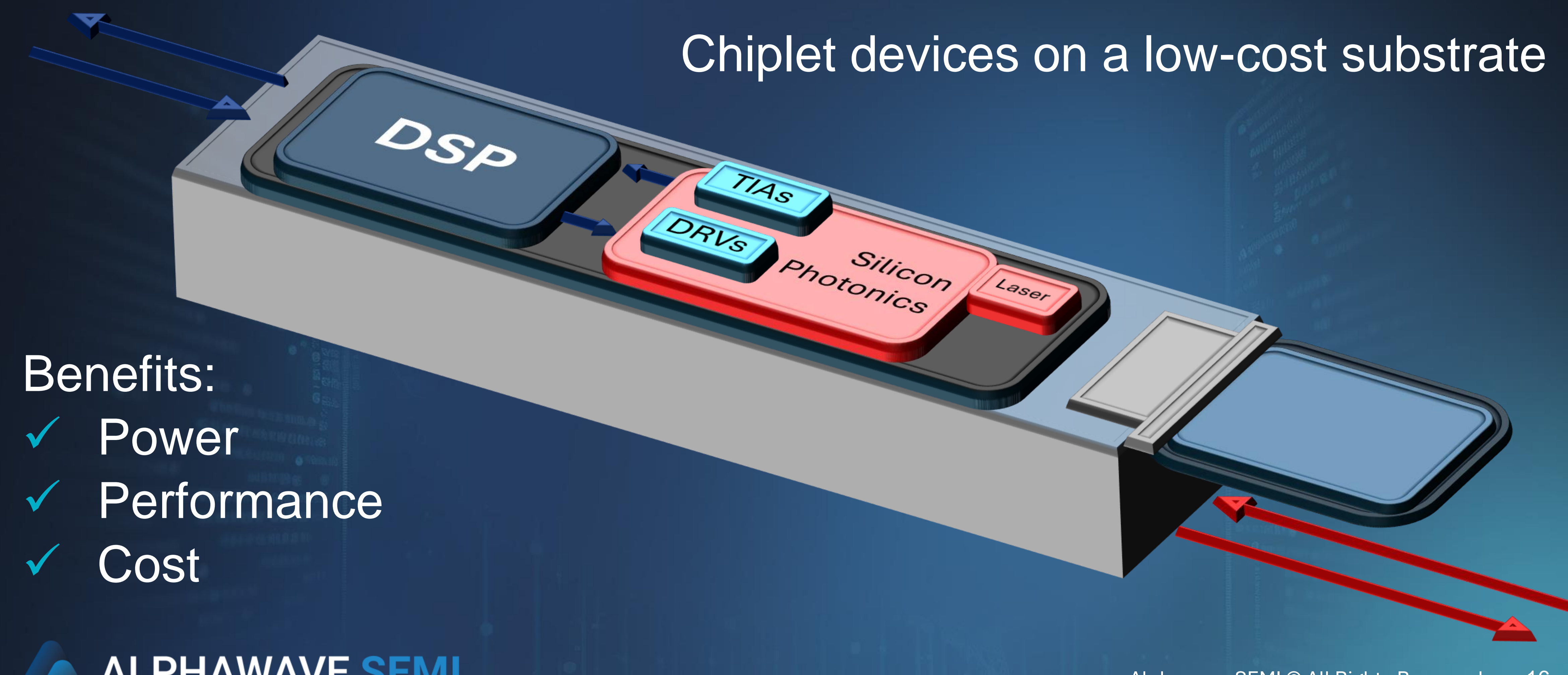
Optical Module Anatomy with Chiplets



Chiplet devices on a low-cost substrate

Benefits:
- ✓ Power
- ✓ Performance
- ✓ Cost

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Co-Packaged Optics (CPO)

Miniature optical engines

Optics
Optics
Optics
Optics
Optics
Optics
ASIC
HBM
HBM
HBM
Package

Optical fiber

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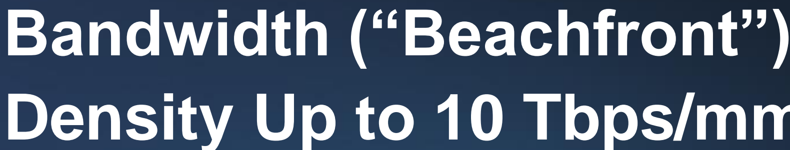
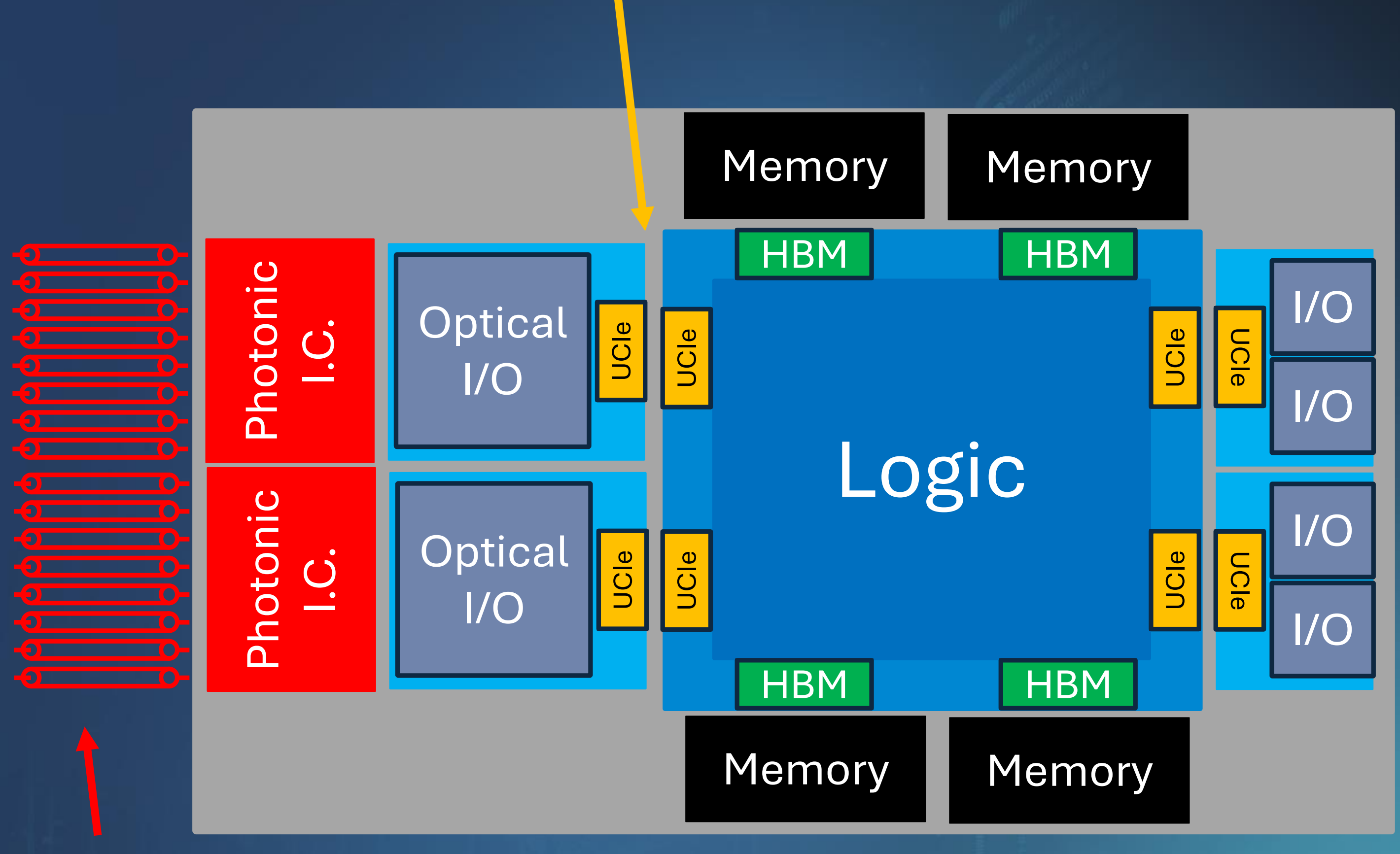
CPO Chiplets



- Mix-and-match with electrical I/O chiplets for different applications
- Optical I/O density being pushed by new solutions:
  - Multiple wavelengths
  - Dense fiber arrays
  - Package fan-out



Beachfront density can be limited by fiber pitch, optical DSP die area

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Distributed Data Centers Driving New Connectivity

Geographically-distributed compute requires broadband connectivity

Coherent-Lite

Future solutions are needed to address these new requirements

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Enabling the Chiplet Ecosystem

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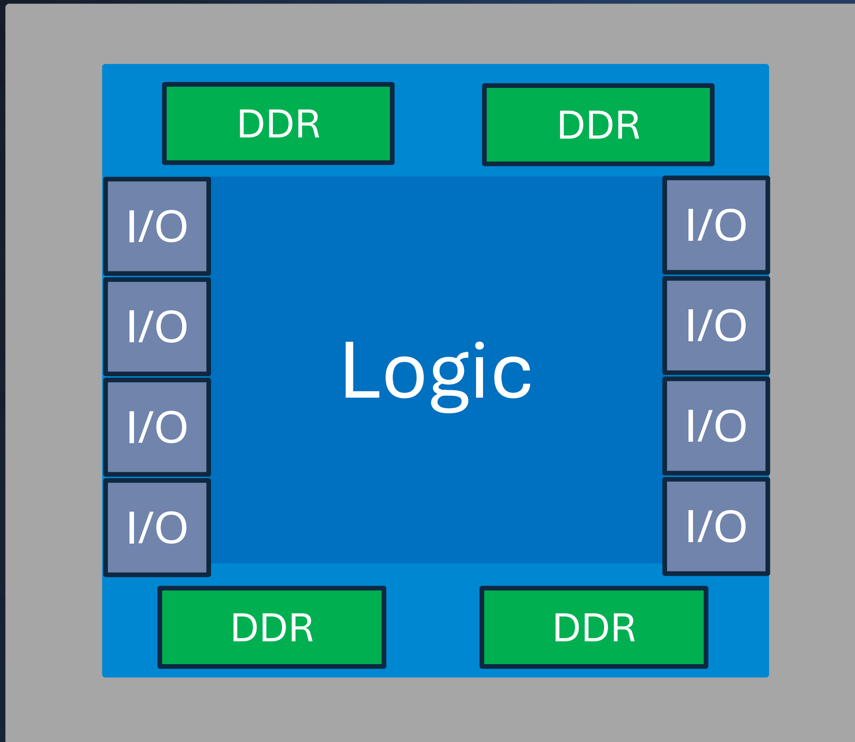
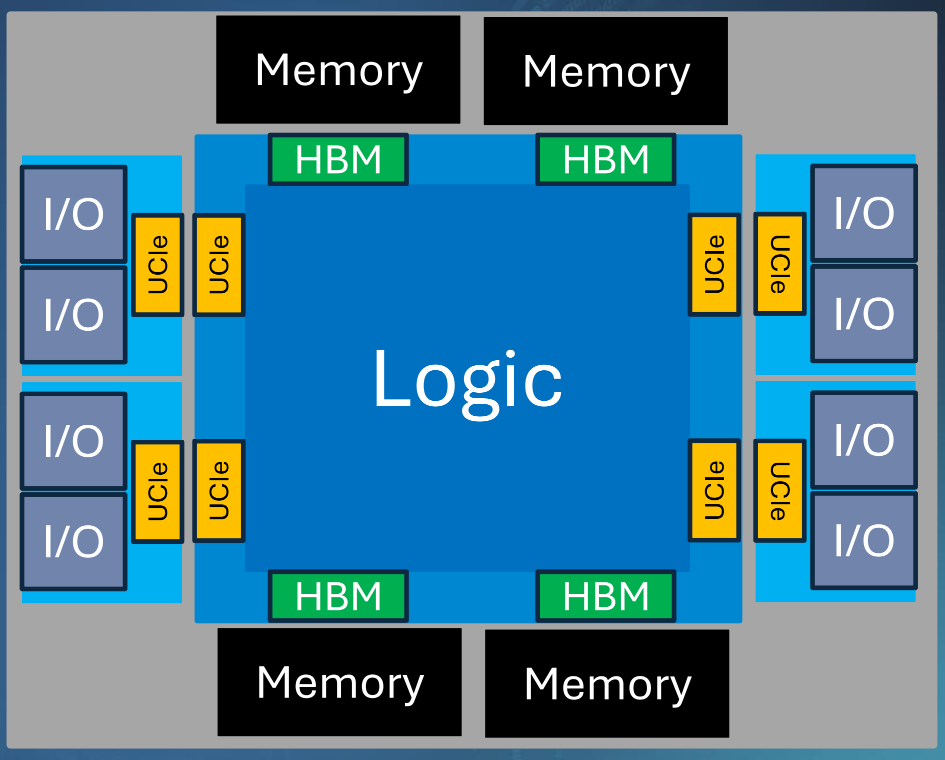
Design Paradigm Transformation

Monolithic Design with Foundry-Enabled Foundation IP

- Accelerated design



- Evolution of Hardware Design



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Die-to-Die Interfaces Supporting a Chiplet Ecosystem

Bandwidth density

Energy efficiency

Latency

Reach

Availability, Interoperability, Reliability

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Key Technologies in Die-to-Die Interfaces

Signal Integrity

- Managing Crosstalk
- Interconnect loss compensation

Power Integrity

- Limited area for supply decoupling
- Variation in packaging technology and dense signal routing complicate power delivery

Clocking

- Low-power and low-jitter clock distribution
- Clock/Data alignment

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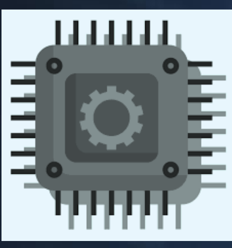
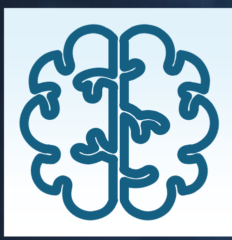
A Chiplet Portfolio

- I/O Chiplet
  - **Multi-Standard SerDes IO with Integrated Protocol Controllers: PCIe Gen6 / CXL 3.0 / 112Gbps Ethernet**



- Compute Chiplet
  - **High Performance, Arm-Based Compute**



- Memory Expansion Chiplet
  - **Low Latency DDR/HBM**

➢ **UCIe Die-to-Die Interfaces**

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Takeaways

- **AI has redefined datacenter infrastructure**
- Connectivity technologies are the key to scaling AI clusters and geographically distributed datacenters effectively
- **Chiplets enable custom silicon solutions optimized for AI workloads**
- Essential to affordably scale performance, achieve lower power, and faster time to market
- **A chiplet ecosystem is emerging, enabled by die-to-die interfaces** and allowing for a wide variety of chiplet use cases

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Thank You!

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